

ABSTRACT OF THE DISCLOSURE

An image processing apparatus provides a numerical signal generation unit for sequentially generating and outputting regular binary numerical signals in synchronism with a clock signal, a bit exchange unit for generating and outputting, from the output signal of the numerical signal generation unit being managed as an input signal, a signal that order of bits in the input signal has been exchanged or a signal that the bits in the input signal have been reversed, a control unit for controlling the bit order exchange operation or the bit reversal operation of the bit exchange unit, and a storage unit for storing image data, and in the apparatus the image data divided into pixel data and one-dimensionally arranged and stored in the storage unit is read and output in synchronism with the sequential operation of the numerical signal generation unit, and the output signal generated by the bit exchange unit is read and output as an address signal, whereby a rotation/reversal process to a former image is performed. Thus, a circuit size for the image rotation/reversal process can be easily minimized, an operation clock frequency of the apparatus can be easily increased as a whole to achieve a high-speed operation, and also circuit's extendibility and diversion are excellent. Further, since positional information before and after the rotation or the

reversal of each of the plural blocks is considered, a processing time necessary for the image rotation/reversal process can be shortened, and at the same time parallel operations can be achieved.